

**WHAT IS CLAIMED IS: \_\_**

- 1           1. A multi-service circuit which receives information-bearing cells  
2   on an external interface, the multi-service circuit being controlled by a  
3   processor, the multi-service circuit comprising:  
4           plural service devices handling differing telecommunication  
5   services;  
6           a multiplexer/demultiplexer core connected between the plural  
7   service devices and the external interface, the core having a downstream  
8   side for transmitting cells from the external interface to the service devices  
9   and an upstream side for transmitting cells from the service devices to the  
10   external interface, the downstream side having a downstream demultiplexer  
11   and a downstream multiplexer,  
12           wherein the downstream demultiplexer serves to route cells received  
13   from the external interface either:  
14               (1) to an input of the downstream multiplexer; or  
15               (2) to one of:  
16                   (a) a downstream loop back buffer which stores cells  
17                   routed from the downstream side to the upstream side, and  
18                   (b) the processor.

1                   2. The apparatus of claim 1, wherein the downstream  
2 multiplexer serves to obtain cells from either:

3                   (1) the downstream demultiplexer, or

4                   (2) one of:

5                   (a) an upstream loop-back buffer which stores cells  
6 routed from the upstream side to the downstream side, and

7                   (b) the processor,

8 for transmission to the service devices.

1                   3. The apparatus of claim 2, wherein the downstream demultiplexer  
2 and the downstream multiplexer are capable of independent simultaneous  
3 operation except when cells are routed from the downstream demultiplexer  
4 to the downstream multiplexer.

1                   4. The apparatus of claim 1, wherein the upstream side has an  
2 upstream demultiplexer and an upstream multiplexer, and

3                   wherein the upstream demultiplexer serves to route cells  
4 received from the service devices to one of:

5                   (1) a buffering section situated between the upstream  
6 demultiplexer and the upstream multiplexer: and

7                   (2) either:

8                   (a) the upstream loop-back buffer, or

9                   (b) the processor.

1           5. The apparatus of claim 1, wherein the upstream demultiplexer  
2 serves to route cells received from the service devices and from the  
3 processor to one of:

4                   (1) the buffering section situated between the upstream  
5 demultiplexer and the upstream multiplexer; and

6                   (2) either:

7                           (a) the upstream loop-back buffer, or

8                           (b) the processor.

1           6. The apparatus of claim 4, wherein the upstream multiplexer  
2 serves to obtain cells from one of the buffering section and the downstream  
3 loop-back buffer for application to the external interface.

1           7. The apparatus of claim 1, wherein at least one of the service  
2 devices is an ATMF transceiver.

1           8. The apparatus of claim 1, wherein at least one of the service  
2 devices is an emulator which interfaces with one of: (1) a PCM interface;  
3 (2) a E1 interface; and (3) a T1 interface.

1           9. The apparatus of claim 8, wherein the emulator has a buffer  
2 which is either totally filled or partially filled with data from one channel.

1           10. The apparatus of claim 8, wherein the emulator has a buffer  
2 which is either totally filled or partially filled with data from all channels.

1           11. The apparatus of claim 1, wherein at least one of the service  
2 devices is a Utopia 2 level device.

1           12. The apparatus of claim 1, wherein the cells are ATM cells.

1           13. The apparatus of claim 1, wherein a Utopia level 2 tributary  
2 interface connects the plural service devices to the  
3 multiplexer/demultiplexer core.

1           14. The apparatus of claim 1, wherein the multi-service circuit is  
2 formed as an integrated chip.

1           15. The apparatus of claim 1, wherein the multi-service circuit is  
2 formed entirely by hardware.

1           16. A multi-service circuit which receives information-bearing cells  
2 on an external interface, the multi-service circuit being controlled by a  
3 processor, the multi-service circuit comprising:

4           plural service devices handling differing telecommunication  
5 services;

6           a multiplexer/demultiplexer core connected between the plural  
7 service devices and the external interface, the core having a downstream  
8 side for transmitting cells from the external interface to the service devices  
9 and an upstream side for transmitting cells from the service devices to the  
10 external interface, the upstream side having an upstream multiplexer and an  
11 upstream demultiplexer,

12 wherein the upstream demultiplexer serves to route cells  
13 received from the service devices to one of:

14 (1) a buffering section situated between the upstream  
15 demultiplexer and the upstream multiplexer; and

16 (2) either:

17 (a) an upstream loop-back buffer which routes cells  
18 from the upstream side to the downstream side, or

19 (b) the processor.

1 17. The apparatus of claim 16, wherein the upstream demultiplexer  
2 serves to route cells received from the service devices and from the  
3 processor to one of:

4 (1) the buffering section situated between the upstream  
5 demultiplexer and the upstream multiplexer; and

6 (2) either:

7 (a) the upstream loop-back buffer, or

8 (b) the processor.

1 18. The apparatus of claim 17, wherein the upstream multiplexer  
2 serves to obtain cells from one of the buffering section and the downstream  
3 loop-back buffer for application to the external interface.

1 19. The apparatus of claim 16, wherein at least one of the service  
2 devices is an ATM/F transceiver.

1           20. The apparatus of claim 16, wherein at least one of the service  
2 devices is an emulator which interfaces with one of: (1) a PCM interface;  
3 (2) a E1 interface; and (3) a T1 interface.

1           21. The apparatus of claim 20, wherein the emulator has a buffer  
2 which is either totally filled or partially filled with data from one channel.

1           22. The apparatus of claim 20, wherein the emulator has a buffer  
2 which is either totally filled or partially filled with data from all channels.

1           23. The apparatus of claim 16, wherein at least one of the service  
2 devices is a Utopia 2 level device.

1           24. The apparatus of claim 16, wherein the cells are ATM cells.

1           25. The apparatus of claim 16, wherein a Utopia level 2 tributary  
2 interface connects the plural service devices to the  
3 multiplexer/demultiplexer core.

1           26. The apparatus of claim 16, wherein the multi-service circuit is  
2 formed as an integrated chip.

1           27. The apparatus of claim 16, wherein the multi-service circuit is  
2 formed entirely by hardware.

1           28. A multi-service circuit which receives ATM cells on an  
2 external interface from a modem/transceiver, the multi-service circuit being  
3 controlled by a processor, the multi-service circuit comprising:  
4           plural service devices handling differing telecommunication  
5 services;  
6           a multiplexer/demultiplexer core connected between the plural  
7 service devices and the external interface, the core having:  
8           a downstream side for transmitting cells from the external  
9 interface to the service devices and an upstream side for transmitting cells  
10 from the service devices to the external interface, the downstream side  
11 having a downstream demultiplexer and a downstream multiplexer, the  
12 upstream side having an upstream multiplexer and an upstream  
13 demultiplexer,  
14           a downstream loop-back buffer for storing cells routed from  
15 the downstream side to the upstream side;  
16           an upstream loop-back buffer for storing cells routed from the  
17 upstream side to the downstream side;  
18           wherein the downstream demultiplexer serves to route cells  
19 received from the external interface to one of the downstream loop back  
20 buffer, the processor, and an input of the downstream multiplexer;  
21           wherein the downstream multiplexer serves to obtain cells  
22 from one of the downstream demultiplexer, the upstream loop-back buffer,  
23 and the processor for transmission to the service devices;  
24           wherein the upstream demultiplexer serves to route cells  
25 received from the service devices and from the processor to one of the

26 upstream loop-back buffer, the processor, and a buffering section situated  
27 between the upstream demultiplexer and the upstream multiplexer; and  
28 wherein the upstream multiplexer serves to obtain cells from one of  
29 the buffering section and the downstream loop-back buffer for application  
30 to the external interface.

1 29. The apparatus of claim 28, wherein the downstream  
2 demultiplexer and the downstream multiplexer are capable of independent  
3 simultaneous operation except when cells are routed from the downstream  
4 demultiplexer to the downstream multiplexer.

1 30. The apparatus of claim 29, wherein at least one of the service  
2 devices is an ATMF transceiver.

1 31. The apparatus of claim 29, wherein at least one of the service  
2 devices is an emulator which interfaces with one of: (1) a PCM interface;  
3 (2) a E1 interface; and (3) a T1 interface.

1 32. The apparatus of claim 31, wherein the emulator has a buffer  
2 which is either totally filled or partially filled with data from one channel.

1 33. The apparatus of claim 31, wherein the emulator has a buffer  
2 which is either totally filled or partially filled with data from all channels.

1 34. The apparatus of claim 29, wherein at least one of the service  
2 devices is a Utopia 2 level device.



1           35. The apparatus of claim 29, wherein the cells are ATM cells.

1           36. The apparatus of claim 29, a Utopia level 2 tributary interface  
2 connects the plural service devices to the multiplexer/demultiplexer core.

1           37. The apparatus of claim 29, wherein the multi-service circuit is  
2 formed as an integrated chip.

1           38. The apparatus of claim 29, wherein the multi-service circuit is  
2 formed entirely by hardware.

1           39. A multi-service circuit which receives ATM cells on an external  
2 interface from a modem/transceiver, the multi-service circuit being  
3 controlled by a processor, the multi-service circuit being fabricated as an  
4 chip and comprising:

5           plural service devices handling differing telecommunication  
6 services;

7           a multiplexer/demultiplexer core connected between the plural  
8 service devices and the external interface;

9           an internal interface connecting the core to the plural service  
10 devices; and

11          wherein, in a downstream direction, the core routes cells received  
12 from the external interface to one of the plural service devices via the  
13 internal interface, to the processor, and to the external interface;

14            wherein, in an upstream direction, the core routes cells received  
15    from the plural service devices via the internal interface and the processor  
16    to one of the external interface, to the processor, and to the internal  
17    interface.

1            40. The apparatus of claim 39, wherein at least one of the external  
2    interface and the internal interface are a Utopia level 2 interface.

1            41. The apparatus of claim 39, wherein the multi-service circuit is  
2    formed entirely by hardware.